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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,372	11/21/2001	Richard H. Lane	M4065.0338/P338-A	1348

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,372	LANE, RICHARD H.	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-32,34-39,41,44-47,49 and 51-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29-32,34 and 35* is/are allowed.

6)☒ Claim(s) *36-39, 41, 44-47, 49 and 51-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 36-39, 41, 44-47, 49 and 51-64 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 55-58 and 60-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. (U.S. 6,297,527 B1) in view of Aoki et al. (U.S. 6,033,953).

Regarding claims 55-58, Agarwal (see Figures 1-8) discloses a container capacitor comprising: a platinum lower electrode provided within a first insulating layer, the platinum lower electrode comprising a metal layer having a bottom wall and vertical sidewalls extending rectangular upwardly (see Figures 1-8), wherein the platinum metal layer has a thickness of approximately 100-500 angstroms (see Figures 1-8); a second insulating layer provided over the metal layer and in contact with the first insulating layer

and an upper electrode provided over the second insulating layer. Agarwal teaches the above outlined features except for mentioning using an electropolishing method. However, Aoki (see Figure 6) teaches the forming of a capacitor bottom electrode 38 by using an electropolishing method (see column 5, lines 41-42). The electropolishing method would increase the radius of curvature at the extreme end of the metal particle for reducing the leakage current of the capacitor (see column 8, lines 14-17). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use the electropolishing method for forming an electropolished patterned metal layer of Agarwal because such electropolishing method for forming electropolished patterned metal layer would reduce the leakage current of the capacitor, as taught by Aoki (see column 8, lines 15-17).

Regarding claims 60-64, Agarwal (see Figures 1-8) discloses a container capacitor comprising: an insulating layer provided over a substrate; a plurality of rectangular (see Figures 1-8) opening provided in the insulating layer; and a plurality of platinum lower capacitor electrodes provided along the bottom and sidewalls of respective ones of the rectangular openings, the platinum lower electrodes being formed as discrete metal layers, wherein the platinum electrodes have a thickness of approximately 100-500 angstroms (see Figures 1-8); and a dielectric layer associated with each of the discrete the platinum lower electrodes, the dielectric layer being in contact with the first insulating layer. Agarwal teaches the above outlined features except for mentioning using an electropolishing method. However, Aoki (Fig. 6) teaches the forming of a capacitor bottom electrode 38 by using an electropolishing method (see

column 5, lines 41-42). The electropolishing method would increase the radius of curvature at the extreme end of the metal particle for reducing the leakage current of the capacitor (see column 8, lines 14-17). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use the electropolishing method for forming an electropolished patterned metal layer of Agarwal because such electropolishing method for forming electropolished patterned metal layer would reduce the leakage current of the capacitor, as taught by Aoki (see column 8, lines 15-17).

Claims 36-39, 41, 44-47, 49, 51-54 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. (U.S. 6,297,527 B1) in view of Aoki et al. (U.S. 6,033,953) and further in view of Huang (U.S. Pat. 6,127,260).

Regarding claims 36-39 and 41, Agarwal (see Figures 1-8) discloses a memory cell comprising:

a transistor (not shown) including a gate fabricated on the semiconductor substrate and including a source/drain region in the semiconductor substrate disposed adjacent to the gate (figure 6a);

a platinum metal layer within an insulating layer provided over the substrate wherein a thickness of approximately 100-500 angstroms (see Figures 1-8); and

a container capacitor including a lower electrode, a dielectric layer over the lower electrode, and an upper electrode over the dielectric layer, the lower electrode having a surface aligned over the source/drain region, the platinum metal layer forming the

platinum lower electrode, and the dielectric layer being in contact with the insulating layer.

However, Aoki (see Figure 6) teaches the forming of a capacitor bottom electrode 38 by using an electropolishing method (see column 5, lines 41-42). The electropolishing method would increase the radius of curvature at the extreme end of the metal particle for reducing the leakage current of the capacitor (see column 8, lines 14-17). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use the electropolishing method for forming an electropolished patterned metal layer of Agarwal because such electropolishing method for forming electropolished patterned metal layer would reduce the leakage current of the capacitor, as taught by Aoki (see column 8, lines 15-17).

Agarwal does not teach an upper electrode comprising doped polysilicon. However, Huang (see Figure 4) discloses an upper electrode 35 comprising doped polysilicon (see column 5, lines 51-59). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form dope polysilicon for an upper electrode of Agarwal because such the doped polysilicon of the upper electrode is conventional material used for storage node contacts structure, as taught by Huang.

Regarding claims 44-47 and 49, Agarwal (see Figures 1-8) discloses a processor-based system comprising:

a processor; and

an integrated circuit coupled to the processor, at least one of the integrated circuit and processor comprising a container capacitor provided within an insulating layer, the container capacitor including a platinum lower electrode having a thickness of approximately 50-300 angstroms (see Figures 1-8), wherein a top surface of the metal layer is at the same level with a top surface of the insulating layer.

However, Aoki (see Figure 6) teaches the forming of a capacitor bottom electrode 38 by using an electropolishing method (see column 5, lines 41-42). The electropolishing method would increase the radius of curvature at the extreme end of the metal particle for reducing the leakage current of the capacitor (see column 8, lines 14-17). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use the electropolishing method for forming an electropolished patterned metal layer of Agarwal because such electropolishing method for forming electropolished patterned metal layer would reduce the leakage current of the capacitor, as taught by Aoki (see column 8, lines 15-17).

Agarwal does not teach an upper electrode comprising doped polysilicon. However, Huang (see Figure 4) discloses an upper electrode 35 comprising doped polysilicon (see column 5, lines 51-59). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form dope polysilicon for an upper electrode of Xing because such the doped polysilicon of the upper electrode is conventional material used for storage node contacts structure, as taught by Huang.

Regarding claims 51-54, Agarwal et al. further teach the integrated circuit may be used in DRAMs, FRAMs and other types of integrated circuits (see Figures 1-8).

Regarding claim 59, as discussed above, Agarwal (see Figures 1-8) further discloses a container capacitor comprising: a tantalum nitride barrier conductive layer.

Allowable Subject Matter

Claims 29-32 and 34-35 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior art of record fails to disclose all the limitations recited in the independent claim. Specifically, the prior art of record fails to disclose an intermediate semiconductor device structure comprising: a photo-resist plug provided within the opening and over and in contact with the electropolished patterned metal layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chuong Anh Luu
Patent Examiner
June 30, 2006